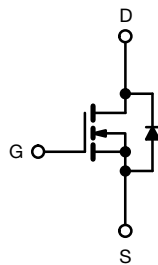
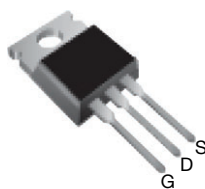


Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Logic-level gate drive
- $R_{DS(on)}$ specified at $V_{GS} = 4\text{ V}$ and 5 V
- $175\text{ }^{\circ}\text{C}$ operating temperature
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5.0\text{ V}$	0.27
Q_g (Max.) (nC)	12	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	7.1	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRL520PbF
Lead (Pb)-free and halogen-free	IRL520PbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	100	V
Gate-source voltage			V_{GS}	± 10	
Continuous drain current	V_{GS} at 5 V	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	9.2	A
		$T_C = 100\text{ }^{\circ}\text{C}$		6.5	
Pulsed drain current ^a			I_{DM}	36	
Linear derating factor				0.40	W/ $^{\circ}\text{C}$
Single pulse avalanche energy ^b			E_{AS}	170	mJ
Repetitive avalanche current ^a			I_{AR}	9.2	A
Repetitive avalanche energy ^a			E_{AR}	6.0	mJ
Maximum power dissipation	$T_C = 25\text{ }^{\circ}\text{C}$		P_D	60	W
Peak diode recovery dV/dt ^c			dV/dt	5.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Soldering recommendations (peak temperature) ^d	For 10 s			300 ^d	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 3.0\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 9.2\text{ A}$ (see fig. 12)
- $I_{SD} \leq 9.2\text{ A}$, $dI/dt \leq 110\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

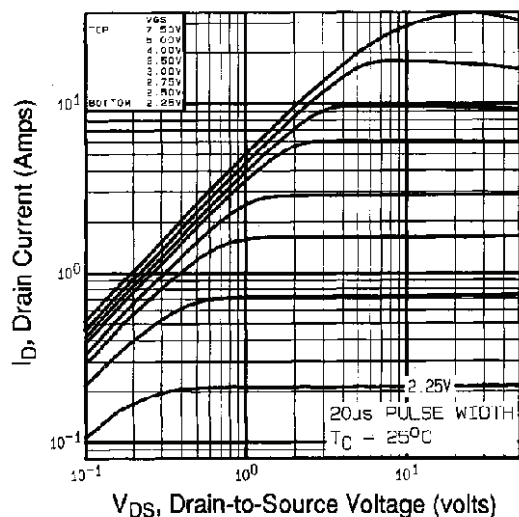
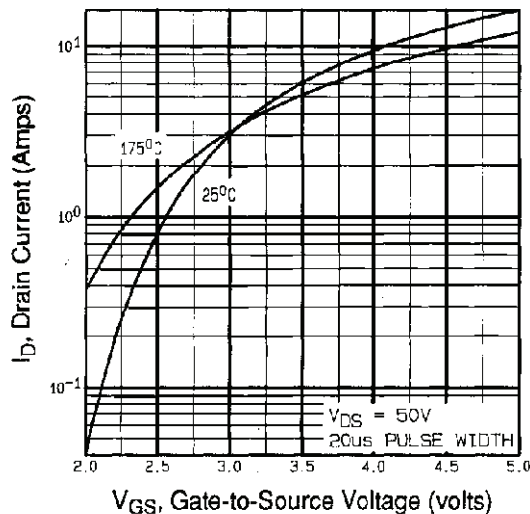
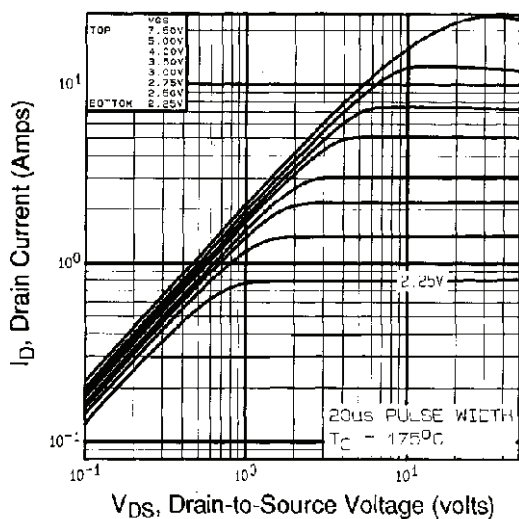
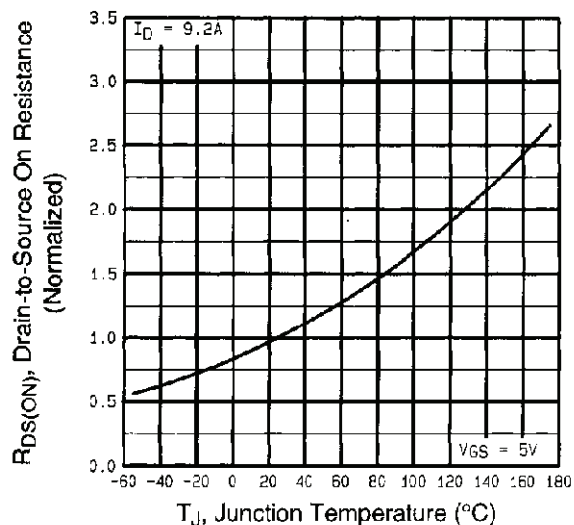
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	2.5	

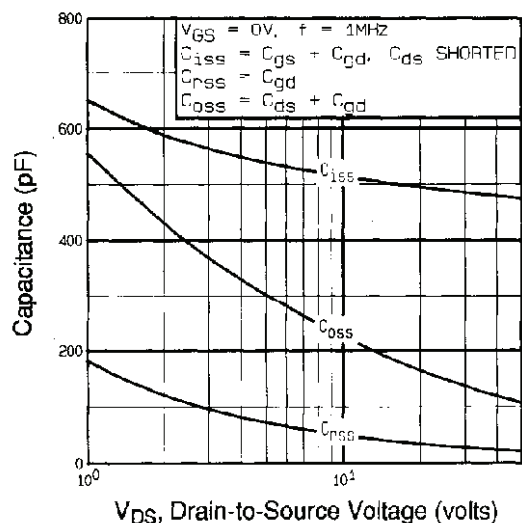
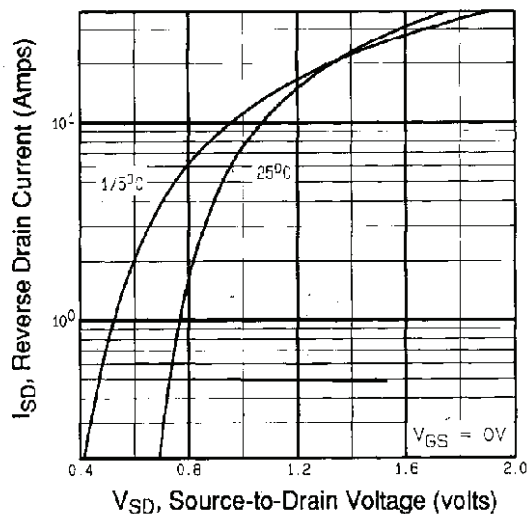
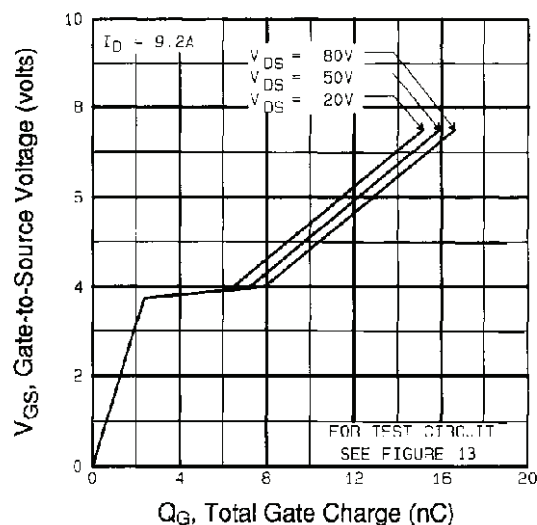
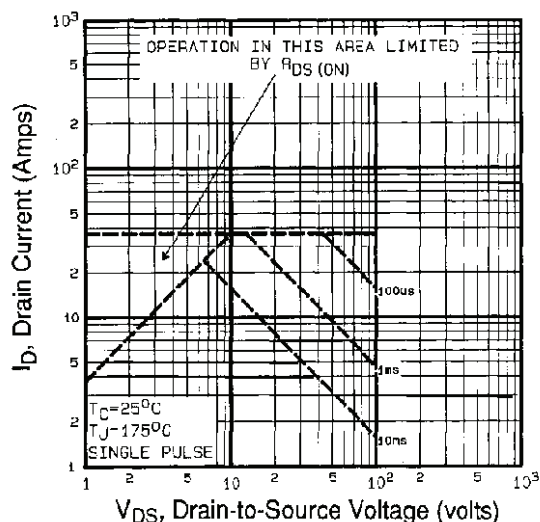
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

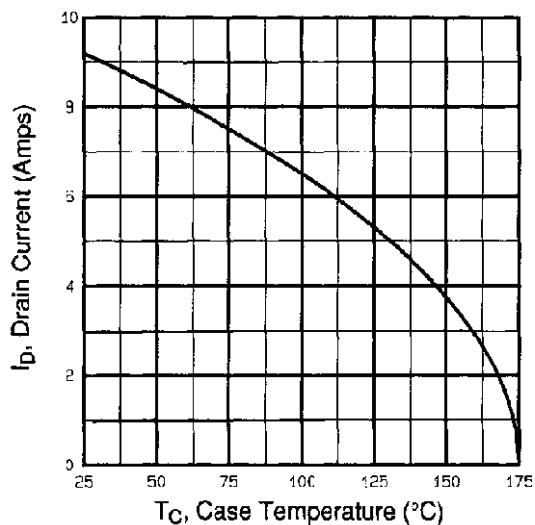
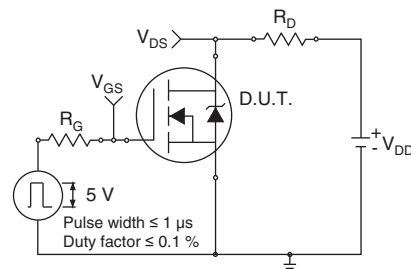
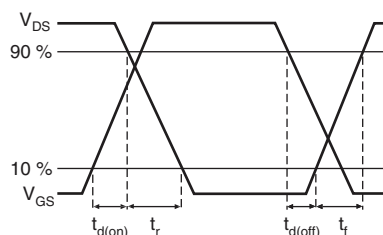
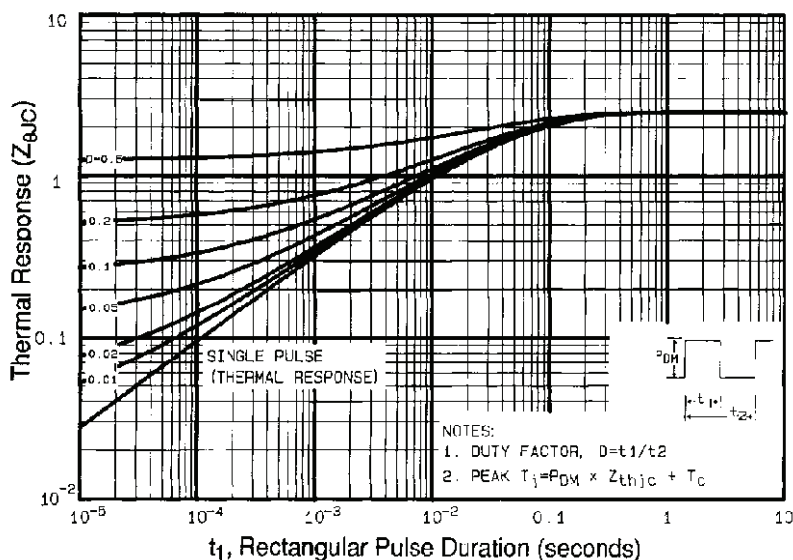
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		100	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.12	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.0	-	2.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 10 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 5.0 V	I _D = 5.5 A ^b	-	-	0.27	Ω
		V _{GS} = 4.0 V	I _D = 4.6 A ^b	-	-	0.38	
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 5.5 A		3.2	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	490	-	pF
Output capacitance	C _{oss}			-	150	-	
Reverse transfer capacitance	C _{rss}			-	30	-	
Total gate charge	Q _g	V _{GS} = 5.0 V	I _D = 9.2 A, V _{DS} = 80 V, see fig. 6 and 13 ^b	-	-	12	nC
Gate-source charge	Q _{gs}			-	-	3.0	
Gate-drain charge	Q _{gd}			-	-	7.1	
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, I _D = 9.2 A, R _g = 9.0 Ω, R _D = 5.2 Ω, see fig. 10 ^b		-	9.8	-	ns
Rise time	t _r			-	64	-	
Turn-off delay time	t _{d(off)}			-	21	-	
Fall time	t _f			-	27	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	9.2	A
Pulsed diode forward current ^a	I _{SM}			-	-	36	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 9.2 A, V _{GS} = 0 V ^b		-	-	2.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 9.2 A, dI/dt = 100 A/μs ^b		-	130	190	ns
Body diode reverse recovery charge	Q _{rr}			-	0.83	1.0	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

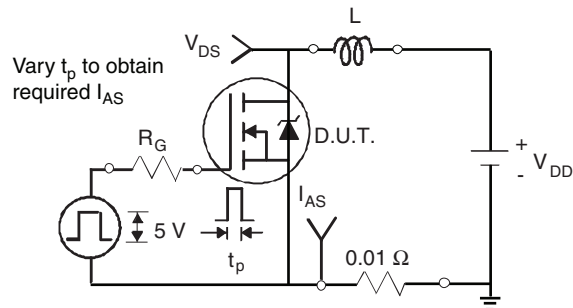
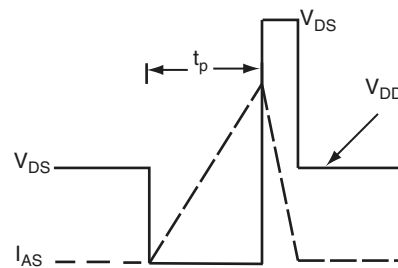
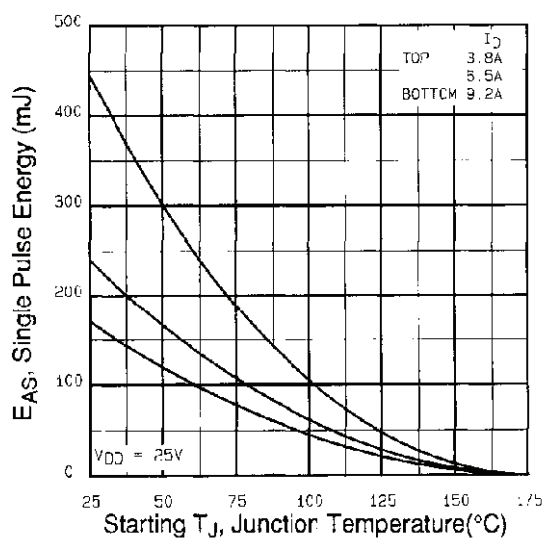
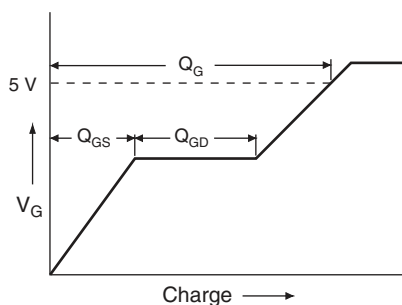
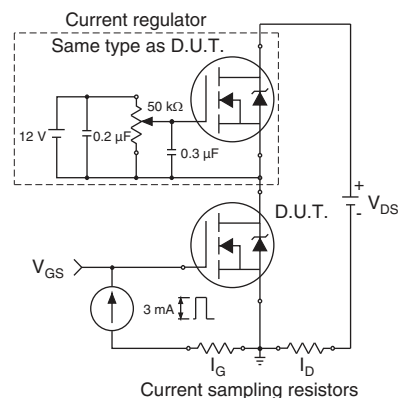
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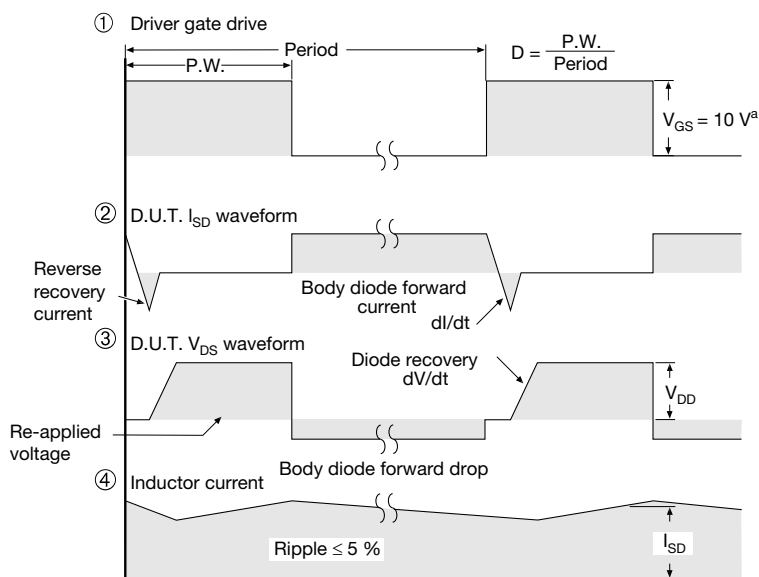
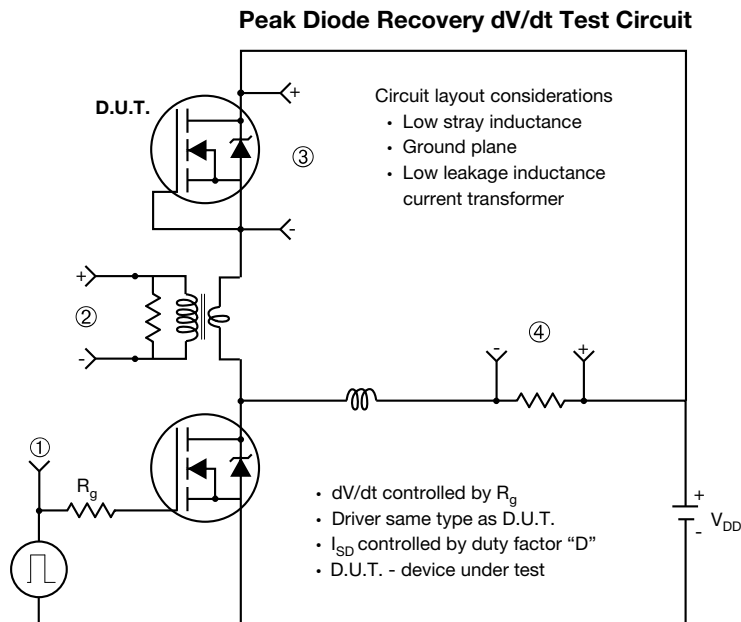
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^{\circ}\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Safe Operating Area

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

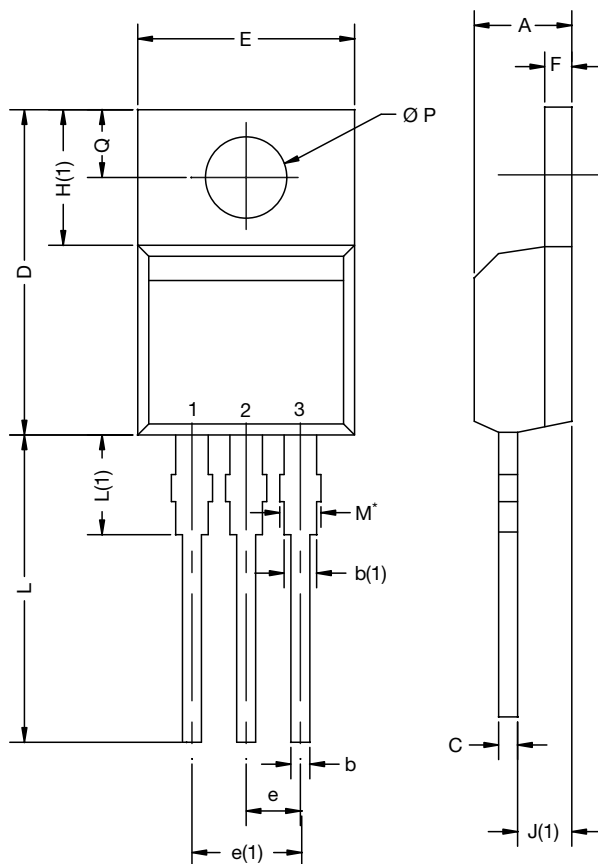

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
$\varnothing P$	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021
DWG: 6031

Note

- M^* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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